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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,875	09/29/2003	Mahesh J. Deshmane	42P17507	6817

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,875	DESHMANE ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003 and 09 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received March 9, 2006 for application number 10/675875 originally filed September 29, 2003. The cancelled claims, 2, 12 and 23, have been noted.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, 5, 10, 11, 22 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ware et al. (U.S. Patent Publication No. 2004/0054845 A1) (hereinafter referred to as Ware).

As to claim 1, Ware discloses a computer system comprising: a bus (DQ bus 3620); and a chipset (memory controller 3601), coupled to the bus, having: a slew rate detection mechanism (calibration process completed by pre-driver within the output transmitter 3603 of memory controller 3601) to detect (measure) the slew rate and generate (Ware discloses adjusting the slew rate which necessitates a signal being generated to indicate the status of the signal) a signal to indicate the status of the slew rate (Ware discloses the pre-driver of the output transmitter [3603] within the memory controller [3601] including circuitry to control the slew rate of the driver wherein a calibration process is completed to measure the slew rate and transfer characteristics and adjusting said slew rate to achieve optimal transfer characteristics; paragraphs 325 and 332); and, control logic (Though not shown, Ware discloses the pre-driver of the output transmitter [3603] having the ability to control the slew rate which necessitates a control logic),

coupled to the slew rate detection mechanism, to receive (Ware discloses the calibration process adjusting the slew rate which necessitates an adjustment signal being received) the signal and modify (adjust) the slew rate based upon the signal (paragraph 332, lines 19-35 and paragraphs 333 and 334).

As to claim 4, Ware discloses the computer system wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast (Ware discloses the optimizing transmission of the signal by adjusting various transfer characteristics for the slew rate which necessitates increasing or reducing of the slew rate; paragraph 332, lines 19-35 and paragraphs 333 and 334).

As to claim 5, Ware discloses the computer system wherein the control logic increases the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too slow (Ware discloses the optimizing transmission of the signal by adjusting various transfer characteristics for the slew rate which necessitates increasing or reducing of the slew rate; paragraph 332, lines 19-35 and paragraphs 333 and 334).

As to claim 10, Ware discloses a computer system wherein the bus is a high-speed bus (Ware discloses a memory system wherein high performance is maintained; paragraph 55).

As to claim 11, Ware discloses a computer system comprising: a main memory device (figure 27 and paragraphs 64-65); a memory bus (2708 of figure 27 or 3620 of figure 36) coupled to the main memory device (paragraph 254); and a memory controller (2702 of figure 27 or 3601 of figure 36), coupled to the bus, having: a slew rate detection mechanism (calibration process completed by pre-driver within the output transmitter 3603 of memory controller 3601) to detect (measure) the slew rate and generate (Ware discloses adjusting the slew rate which

necessitates a signal being generated to indicate the status of the signal) a signal to indicate the status of the slew rate (Ware discloses the pre-driver of the output transmitter [3603] within the memory controller [3601] including circuitry to control the slew rate of the driver wherein a calibration process is completed to measure the slew rate and transfer characteristics and adjusting said slew rate to achieve optimal transfer characteristics; paragraphs 325 and 332); and, control logic (Though not shown, Ware discloses the pre-driver of the output transmitter [3603] having the ability to control the slew rate which necessitates a control logic), coupled to the slew rate detection mechanism, to receive (Ware discloses the calibration process adjusting the slew rate which necessitates an adjustment signal being received) the signal and modify (adjust) the slew rate based upon the signal (paragraph 332, lines 19-35 and paragraphs 333 and 334).

As to claim 13, Ware discloses the computer system wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast (Ware discloses the optimizing transmission of the signal by adjusting various transfer characteristics for the slew rate which necessitates increasing or reducing of the slew rate; paragraph 332, lines 19-35 and paragraphs 333 and 334).

As to claim 14, Ware discloses the computer system wherein the control logic increases the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too slow (Ware discloses the optimizing transmission of the signal by adjusting various transfer characteristics for the slew rate which necessitates increasing or reducing of the slew rate; paragraph 332, lines 19-35 and paragraphs 333 and 334).

As to claim 22, Ware discloses an apparatus comprising: a slew rate detection mechanism (calibration process completed by pre-driver within the output transmitter 3603 of memory

controller 3601) to detect (measure) the slew rate of a signal transmitted from a memory controller (Measuring the slew rate necessitates a signal being transmitted over the bus [3620] between components [3601 and 3602]) over a bus (DQ bus 3620) and to generate (Ware discloses adjusting the slew rate which necessitates a signal being generated to indicate the status of the signal) a signal to indicate the status of the slew rate (Ware discloses the pre-driver of the output transmitter [3603] within the memory controller [3601] including circuitry to control the slew rate of the driver wherein a calibration process is completed to measure the slew rate and transfer characteristics and adjusting said slew rate to achieve optimal transfer characteristics; paragraphs 325 and 332).

As to claim 24, Ware discloses the apparatus further comprising control logic (Though not shown, Ware discloses the pre-driver of the output transmitter [3603] having the ability to control the slew rate which necessitates a control logic), coupled to the slew rate detection mechanism, to receive (Ware discloses the calibration process adjusting the slew rate which necessitates an adjustment signal being received) the signal and modify (adjust) the slew rate based upon the signal (paragraph 332, lines 19-35 and paragraphs 333 and 334).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 18, 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (U.S. Patent Publication No. 2004/0054845 A1) (hereinafter referred to as Ware) and Donnelly et al. (U.S. Patent No. 5,959,481) (hereinafter referred to as Donnelly).

As to claim 3, Ware discloses a computer memory system wherein the chipset (driver circuit in figure 36 exemplified by 3608; paragraph 332, lines 8-26) to detect the slew rate of a signal transmitted over the bus via the chipset, and to adjust the slew rate based upon the state of the signal (paragraphs 55 and 61).

Ware fails to disclose the system chipset further comprises an input/output (I/O) buffer coupled to the control logic.

Donnelly teaches a bus driver circuit (200) having slew rate control wherein said driver circuit comprises an I/O buffer (220; column 6, lines 17-21).

It would have been obvious to one of ordinary skill of the art, having the teachings of Ware and Donnelly before him at the time the invention was made, to modify the bus driver circuit disclosed by Ware to include an I/O buffer as taught by Donnelly.

One of ordinary skill in the art would be motivated to make use of bus driver circuit in view of the teachings of Donnelly, as doing so would give the added benefit of having the slew circuits manufactured on the same substrate as surrounding circuit therefore enabling the slew circuitry to track and compensate slew variations as they occur (column 3, lines 50-67).

As to claim 18, Ware discloses a method comprising: receiving (Ware discloses a calibration process adjusting the slew rate which necessitates a signal being transferred between the memory controller [3601] and memory component [3602] to measure said slew rate) a signal at a slew rate detection mechanism (calibration process completed by pre-driver within the

output transmitter 3603 of memory controller 3601) within the chipset (3601) via the bus (DQ bus 3620) (Ware discloses the pre-driver of the output transmitter [3603] within the memory controller [3601] including circuitry to control the slew rate of the driver wherein a calibration process is completed to measure the slew rate and transfer characteristics and adjusting said slew rate to achieve optimal transfer characteristics; paragraphs 325 and 332); generating (Ware discloses adjusting the slew rate which necessitates a signal being generated to indicate the status of the signal) a signal indicating the status of the slew rate (Ware discloses the pre-driver of the output transmitter [3603] within the memory controller [3601] including circuitry to control the slew rate of the driver wherein a calibration process is completed to measure the slew rate and transfer characteristics and adjusting said slew rate to achieve optimal transfer characteristics; paragraphs 325 and 332); and adjusting the slew rate at control logic (Though not shown, Ware discloses the pre-driver of the output transmitter [3603] having the ability to control the slew rate which necessitates a control logic) within the chipset based upon the signal (paragraph 332, lines 19-35 and paragraphs 333 and 334).

Ware fails to disclose transmitting a signal from an input/output (I/O) buffer over a bus; receiving the signal at a slew rate detection mechanism within the chipset via the bus; and generating a signal indicating the status of the slew rate.

Donnelly teaches a bus driver circuit (200) comprising an I/O buffer (220; column 6, lines 17-21), receiving the signal at a slew rate detection mechanism and generating a signal indicating the status of the slew rate (230; column 4, lines 44-65).

It would have been obvious to one of ordinary skill of the art, having the teachings of Ware and Donnelly before him at the time the invention was made, to modify the bus driver circuit disclosed by Ware to use the slew detection method and I/O buffer as taught by Donnelly.

One of ordinary skill in the art would be motivated to make use of bus driver method in view of the teachings of Donnelly, as doing so would give the added benefit of having the slew circuits manufactured on the same substrate as surrounding circuit therefore enabling the slew circuitry to track and compensate slew variations as they occur (column 3, lines 50-67).

As to claim 21, Ware discloses the method wherein adjusting the slew rate comprises modifying the amplification (controlling the strength of the pre-driver transistors) of a second signal at the I/O buffer (paragraphs 333 and 334).

As to claim 25, Ware fails to disclose the apparatus further comprising an input/output (I/O) buffer coupled to the control logic.

Donnelly teaches a bus driver circuit (200) comprising an I/O buffer (220; column 6, lines 17-21), receiving the signal at a slew rate detection mechanism and generating a signal indicating the status of the slew rate (230; column 4, lines 44-65).

It would have been obvious to one of ordinary skill of the art, having the teachings of Ware and Donnelly before him at the time the invention was made, to modify the bus driver circuit disclosed by Ware to use the slew detection method and I/O buffer as taught by Donnelly.

One of ordinary skill in the art would be motivated to make use of bus driver method in view of the teachings of Donnelly, as doing so would give the added benefit of having the slew circuits manufactured on the same substrate as surrounding circuit therefore enabling the slew circuitry to track and compensate slew variations as they occur (column 3, lines 50-67).

Claims 6, 9, 15 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (U.S. Patent Publication No. 2004/0054845 A1) (hereinafter referred to as Ware) and Donnelly et al. (U.S. Patent No. 5,959,481) (hereinafter referred to as Donnelly) as applied to claims 2, 12, 18 and 22 above, and further in view of Lee et al. (U.S. Patent No. 6,614,285 B2) (hereinafter referred to as Lee).

As to claim 6, Ware and Donnelly fail to teach the slew detection mechanism to include a capacitor to integrate the received signal current.

Lee teaches an integrator circuit (figure 2) to include a capacitor (Cin) to integrate the received current on an input terminal (Vin) (Lee teaches the integrator circuit being capable of repairing slew on the signal line; column 4, lines 38-48).

It would have been obvious to one of ordinary skill of the art, having the teachings of Ware, Donnelly and Lee before him at the time the invention was made, to modify the slew detector circuit disclosed by Ware and Donnelly to use the integrator circuit containing a capacitor with slew detection and repair method and as taught by Lee.

One of ordinary skill in the art would be motivated to make use of slew detection circuit in view of the teachings of Lee, as doing so would give the added benefit of achieving low distortion and noise with minimal power consumption (column 2, lines 40-45).

As to claim 9, Donnelly teaches the computer system wherein the comparator (410) is an operational amplifier (column 6, lines 29-31).

As to claim 15, Ware and Donnelly fail to teach the slew detection mechanism to include a capacitor to integrate the received signal current.

Lee teaches an integrator circuit (figure 2) to include a capacitor (Cin) to integrate the received current on an input terminal (Vin) (Lee teaches the integrator circuit being capable of repairing slew on the signal line; column 4, lines 38-48).

It would have been obvious to one of ordinary skill of the art, having the teachings of Ware, Donnelly and Lee before him at the time the invention was made, to modify the slew detector circuit disclosed by Ware and Donnelly to use the integrator circuit containing a capacitor with slew detection and repair method and as taught by Lee.

One of ordinary skill in the art would be motivated to make use of slew detection circuit in view of the teachings of Lee, as doing so would give the added benefit of achieving low distortion and noise with minimal power consumption (column 2, lines 40-45).

As to claim 26, Ware and Donnelly fail to teach the slew detection mechanism to include a capacitor to integrate the received signal current.

Lee teaches an integrator circuit (figure 2) to include a capacitor (Cin) to integrate the received current on an input terminal (Vin) (Lee teaches the integrator circuit being capable of repairing slew on the signal line; column 4, lines 38-48).

It would have been obvious to one of ordinary skill of the art, having the teachings of Ware, Donnelly and Lee before him at the time the invention was made, to modify the slew detector circuit disclosed by Ware and Donnelly to use the integrator circuit containing a capacitor with slew detection and repair method and as taught by Lee.

One of ordinary skill in the art would be motivated to make use of slew detection circuit in view of the teachings of Lee, as doing so would give the added benefit of achieving low distortion and noise with minimal power consumption (column 2, lines 40-45).

Claims 7, 8, 16, 17, 19, 20, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (U.S. Patent Publication No. 2004/0054845 A1) (hereinafter referred to as Ware), Donnelly et al. (U.S. Patent No. 5,959,481) (hereinafter referred to as Donnelly) and Lee et al. (U.S. Patent No. 6,614,285 B2) (hereinafter referred to as Lee) as applied to claims 6, 15 and 26 above, and further in view of Namiki (U.S. Patent No. 4,704,642) (hereinafter referred to as Namiki).

As to claims 7, 16, 19 and 27, Ware, Donnelly and Lee fail to teach the slew detector mechanism further includes: a reference current generator to generate a reference current; and a comparator to compare the received signal current to the reference current.

Namiki teaches a slew detection circuit (47) comprising a variable resistor that provides a variable voltage reference for comparator (56) wherein the reference delivered is dependent on the slew (column 12, lines 12-30).

It would have been obvious to one of ordinary skill of the art, having the teachings of Ware, Donnelly, Lee and Namiki before him at the time the invention was made, to modify the reference to the comparator within the slew detector as disclosed by Ware, Donnelly and Lee to use the variable reference generator as taught by Namiki. Those skilled in the art should know that the relationship between voltage and current are directly proportionate such that V=iR via Ohm's Law. Therefore, given that the invention is claiming a current reference, it is a moot argument to provide this exact mechanism as voltage levels will provide the same action.

One of ordinary skill in the art would be motivated to make use of comparator reference generator in view of the teachings of Namiki, as doing so would given the added benefit of noise reduction in addition to slew repairing (column 3, lines 30-46).

As to claims 8, 17, 20 and 28, Lee teaches the slew rate detection mechanism further includes: a first converter, coupled to the capacitor and the comparator to convert the signal current to a signal voltage; and a second converter, coupled to the reference current generator and the comparator to convert the reference to a reference voltage (As argued above in claims 7, 16 and 27, Lee provides a voltage reference generator thus providing a voltage to the comparator already; column 12, lines 12-30).

Response to Arguments

Applicant's arguments with respect to claims 1-17, 19, 20 and 22-28 have been considered but are moot in view of the new ground(s) of rejection.

As to claims 18 and 21, it appears that the Examiner's explanations in the first Office Action on this limitation were not set forth clearly. As discussed hereinabove, the reformulated rejection under 35 U.S.C. § 103 still uses the original references cited in the first Office Action: Ware et al. (U.S. Patent Publication No. 2004/0054845 A1) and Donnelly et al. (U.S. Patent No. 5,959,481) and is set forth more clearly. The Examiner respectfully finds the Applicant's arguments moot and therefore, the rejection under 35 U.S.C. § 103 stands.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

James Sugent
Patent Examiner, Art Unit 2116
April 19, 2006

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